1.8-V to 5-V DUAL UART WITH 64-BYTE FIFOS

FEATURES

- Larger FIFOs Reduce CPU Overhead
- Programmable Auto-$\overline{RTS}$ and Auto-$\overline{CTS}$
- In Auto-$\overline{CTS}$ Mode, $\overline{CTS}$ Controls the Transmitter
- In Auto-$\overline{RTS}$ Mode, RCV FIFO Contents, and Threshold Control $\overline{RTS}$
- Serial and Modem Control Outputs Drive a RJ11 Cable Directly When Equipment is on the Same Power Drop
- Capable of Running With All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- Up to 48-MHz Clock Rate for up to 3-Mbps (Standard 16× Sampling) Operation, or up to 6-Mbps (Optional 8× Sampling) Operation With V_{CC} = 5 V Nominal
- Up to 32-MHz Clock Rate for up to 2-Mbps (Standard 16× Sampling) Operation, or up to 4-Mbps (Optional 8× Sampling) Operation With V_{CC} = 3.3 V Nominal
- Up to 24-MHz Clock Rate for up to 1.5-Mbps (Standard 16× Sampling) Operation, or up to 3-Mbps (Optional 8× Sampling) Operation With V_{CC} = 2.5 V Nominal
- Up to 16-MHz Clock Rate for up to 1-Mbps (Standard 16× Sampling) Operation, or up to 2-Mbps (Optional 8× Sampling) Operation With V_{CC} = 1.8 V Nominal
- In TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud-Rate Generator Allows Division of Any Input Reference Clock by 1 to $(2^{16} – 1)$ and Generates an Internal 16× Clock
- Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream
- 5-V, 3.3-V, 2.5-V, and 1.8-V Operation
- Independent Receiver Clock Input
- Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled
- Fully Programmable Serial Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 =-, or 2-Stop Bit Generation
  - Baud Generation (DC to 1 Mbit/s)
- False-Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State Output TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, and Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)
- Available in 44-Pin PLCC (FN) or 32-Pin QFN (RHB) Packages
- Each UART's Internal Register Set May Be Written Concurrently to Save Setup Time
- Multifunction ($\overline{MF}$) Output Allows Users to Select Among Several Functions, Saving Package Pins

APPLICATIONS

- Point-of-Sale Terminals
- Gaming Terminals
- Portable Applications
- Router Control
- Cellular Data
- Factory Automation

DESCRIPTION

The TL16C2752 is a speed and functional upgrade of the TL16C2552. Since they are pinout and software compatible, designs can easily migrate from the TL16C2552 to the TL16C2752 if needed. The additional functionality within the TL16C2752 is accessed via an extended register set. Some of the key new features are larger receive and transmit FIFOs, embedded IrDA encoders and decoders, RS-485 transceiver controls, software flow control (Xon/Xoff) modes, programmable transmit FIFO thresholds, extended receive and transmit threshold levels for interrupts, and extended receive threshold levels for flow control halt/resume operation.

The TL16C2752 is a dual universal asynchronous receiver and transmitter (UART). It incorporates the functionality of two independent UARTs: each UART having its own register set and transmit and receive FIFOs. The two UARTs share only the data bus interface and clock source, otherwise they operate independently. Another name for the UART function is asynchronous communications element (ACE), and these terms will be used interchangeably. The bulk of this document describes the behavior of each ACE, with the understanding that two such devices are incorporated into the TL16C2752.

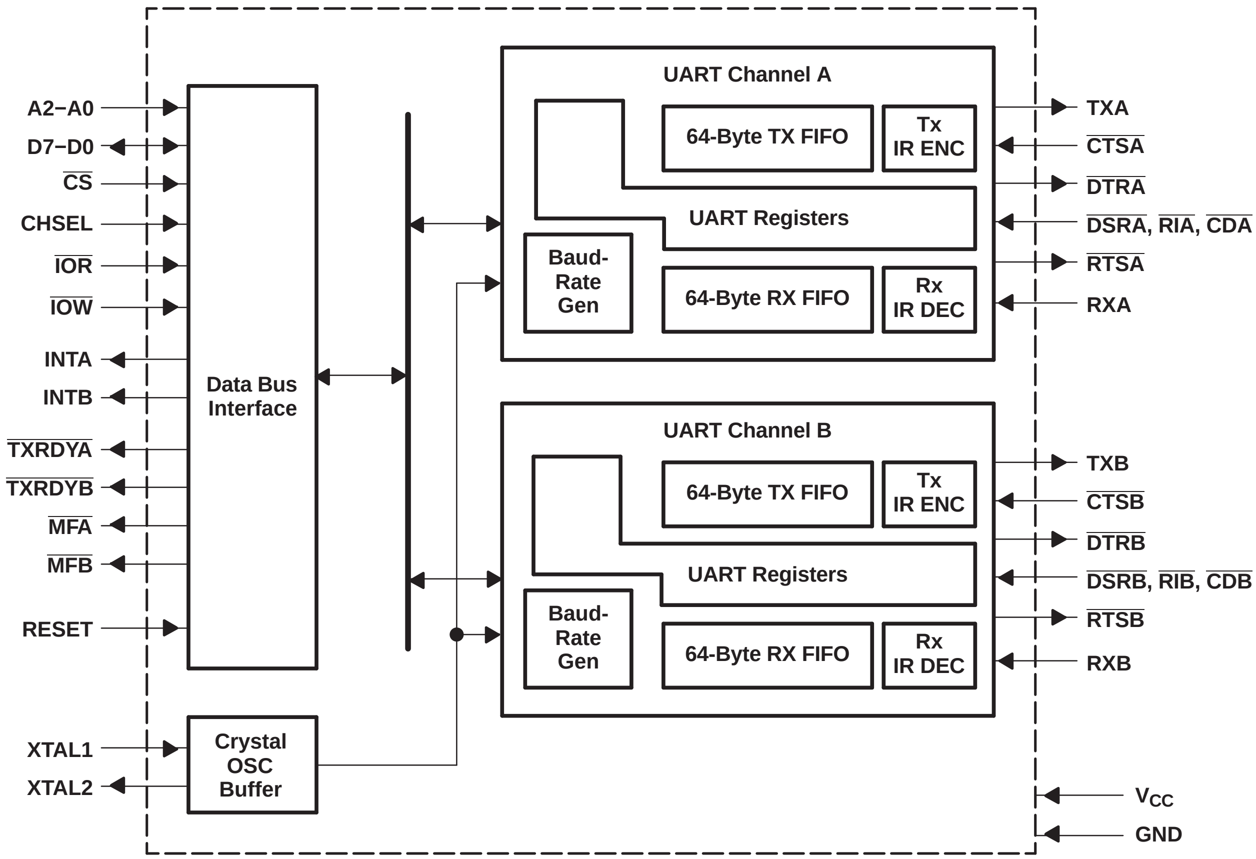
Functionally equivalent to the TL16C450 on power up or reset (single character or TL16C450 mode), each ACE can be placed in an alternate FIFO mode. This relieves the CPU of excessive software overhead by buffering received and to-be-transmitted characters. Each receiver and transmitter store up to 64 bytes in their respective FIFOs, with the receive FIFO including three additional bits per byte for error status. In the FIFO mode, selectable hardware or software autoflow control features can significantly reduce program overload and increase system efficiency by automatically controlling serial data flow.

Each ACE performs serial-to-parallel conversions on data received from a peripheral device or modem and stores the parallel data in its receive buffer or FIFO, and each ACE performs parallel-to-serial conversions on data sent from its CPU after storing the parallel data in its transmit buffer or FIFO. The CPU can read the status of either ACE at any time. Each ACE includes complete modem control capability and a processor interrupt system that can be tailored to the application.

Each ACE includes a programmable baud rate generator capable of dividing a reference clock with divisors of from 1 to 65535, thus producing a 16× or 8× internal reference clock for the transmitter and receiver logic. Each ACE accommodates up to a 3-Mbaud serial data rate (48-MHz input clock). As a reference point, that speed would generate a 333-ns bit time and a 3.33-=s character time (for 8,N,1 serial data), with the internal clock running at 48 MHz and 16× sampling.

Each ACE has a $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ (via $\overline{\text{MF}}$) output that can be used to interface to a DMA controller.

TL16C2752 Block Diagram



A. $\overline{\text{MF}}$ output allows selection of $\overline{\text{OP}}$, $\overline{\text{BAUDOUT}}$, or $\overline{\text{RXRDY}}$ per channel.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	FN NO.	RHB NO.		
A0	10	3	I	Address 0 select bit. Internal registers address selection.
A1	14	6	I	Address 1 select bit. Internal registers address selection.
A2	15	7	I	Address 2 select bit. Internal registers address selection.
$\overline{CDA}$, $\overline{CDB}$	42, 30	–	I	Carrier detect (active low). These inputs are associated with individual UART channels A and B. A low on these pins indicates that a carrier has been detected by the modem for that channel. The state of these inputs is reflected in the modem status register (MSR). These inputs should be pulled high if unused.
CHSEL	16	8	I	Channel select. UART channel A or B is selected by the state of this pin when $\overline{CS}$ is a logic 0. A logic 0 on the CHSEL selects the UART channel B, while a logic 1 selects UART channel A. CHSEL could just be an address line from the user CPU such as A3. Bit 0 of the alternate function register (AFR) can temporarily override CHSEL function, allowing the user to write to both channel register simultaneously with one write cycle when $\overline{CS}$ is low. It is especially useful during the initialization routine.
$\overline{CS}$	18	10	I	UART chip select (active low). This pin selects channel A or B in accordance with the state of the CHSEL pin. This allows data to be transferred between the user CPU and the TL16C2752.
$\overline{CTSA}$, $\overline{CTSB}$	40, 28	25, 17	I	Clear to send (active low). These inputs are associated with individual UART channels A and B. A logic low on the CTS pins indicates the modem or data set is ready to accept transmit data from the TL16C2752. Status can be tested by reading MSR bit 4. These pins only affect the transmit and receive operations when auto CTS function is enabled through the enhanced feature register (EFR) bit 7, for hardware flow control operation. These inputs should be pulled high if unused.
D0–D4 D5–D7	2–6 7–9	27–31 32, 1, 2	I/O	Data bus (bidirectional). These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit (LSB) and the first data bit in a transmit or receive serial data stream.
$\overline{DSRA}$, $\overline{DSRB}$	41, 29	–	I	Data set ready (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem or data set is powered on and is ready for data exchange with the UART. The state of these inputs is reflected in the modem status register (MSR). These inputs should be pulled high if unused.
$\overline{DTRA}$, $\overline{DTRB}$	37, 27	–	O	Data terminal ready (active low). These outputs are associated with individual UART channels A and B. A logic low on these pins indicates that the TL16C2752 is powered on and ready. These pins can be controlled through the modem control register. Writing a 1 to MCR bit 0 sets the $\overline{DTR}$ output to low, enabling the modem. The output of these pins is high after writing a 0 to MCR bit 0, or after a reset.
GND	12, 22	20		Signal and power ground
INTA, INTB	34, 17	21, 9	O	Interrupt A and B (active high). These pins provide individual channel interrupts, INTA and INTB. INTA and INTB are enabled when MCR bit 3 is set to a logic 1, interrupt sources are enabled in the interrupt enable register (IER). Interrupt conditions include receiver errors, available receiver buffer data, available transmit buffer space, or when a modem status flag is detected. INTA and INTB are in the high-impedance state after reset.
$\overline{IOR}$	24	14	I	Read input (active-low strobe). A high-to-low transition on $\overline{IOR}$ loads the contents of an internal register defined by address bits A0–A2 onto the TL16C2752 data bus (D0–D7) for access by an external CPU.
$\overline{IOW}$	20	11	I	Write input (active-low strobe). A low-to-high transition on $\overline{IOW}$ transfers the contents of the data bus (D0–D7) from the external CPU to an internal register that is defined by address bits A0–A2 and $\overline{CSA}$ and $\overline{CSB}$.
NC	–	18, 19		No internal connection
$\overline{MFA}$, $\overline{MFB}$	35, 19	–	O	Multifunction. This output pin can function as the $\overline{OP}$, $\overline{BAUDOUT}$, or $\overline{RXRDY}$ pin. One of these output signal functions can be selected by the user-programmable bits 1–2 of the alternate function register (AFR). These signal functions are described as follows: 1. $\overline{OP}$–When $\overline{OP}$ (active low) is selected, the $\overline{MF}$ pin is a logic 0 when MCR bit 3 is set to a logic 1 (see MCR bit 3). MCR bit 3 defaults to a logic 1 condition after a reset or powerup. 2. $\overline{BAUDOUT}$–When $\overline{BAUDOUT}$ function is selected, the 16× baud rate clock output is available at this pin. 3. $\overline{RXRDY}$–$\overline{RXRDY}$ (active low) is intended for monitoring DMA data transfers. If it is not used, leave it unconnected.

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O	DESCRIPTION
NAME	FN NO.	RHB NO.		
RESET	21	12	I	Reset. RESET will reset the internal registers and all the outputs. The UART transmitter output and the receiver input are disabled during reset time. See TL16C2752 external reset conditions for initialization details. RESET is an active-high input.
$\overline{\text{RIA}}$, $\overline{\text{RIB}}$	43, 31	–	I	Ring indicator (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem has received a ringing signal from the telephone line. A low-to-high transition on these input pins generates a modem status interrupt, if enabled. The state of these inputs is reflected in the modem status register (MSR). These inputs should be pulled high if unused.
$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$	36, 23	22, 13	O	Request to send (active low). These outputs are associated with individual UART channels A and B. A low on the $\overline{\text{RTS}}$ pin indicates the transmitter has data ready and waiting to send. Writing a 1 in the modem control register (MCR bit 1) sets these pins to low, indicating data is available. After a reset, these pins are set to high. These pins only affects the transmit and receive operation when auto $\overline{\text{RTS}}$ function is enabled through the enhanced feature register (EFR) bit 6, for hardware flow control operation.
RXA, RXB	39, 25	24, 15	I	Receive data input. These inputs are associated with individual serial channel data to the TL16C2752. During the local loopback mode, these RX input pins are disabled and TX data is internally connected to the UART RX input internally.
TXA, TXB	38, 26	23, 16	O	Transmit data. These outputs are associated with individual serial transmit channel data from the TL16C2752. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input.
$\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$	1, 32	–	O	Transmit ready (active low). $\overline{\text{TXRDY}}$ A and B go low when there are at least a trigger-level number of spaces available. They go high when the TX buffer is full.
V_{CC}	33, 44	26	I	Power-supply inputs
XTAL1	11	4	I	Crystal or external clock. XTAL1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 4). Alternatively, an external clock can be connected to XTAL1 to provide custom data rates.
XTAL2	13	5	O	Crystal oscillator or buffered clock (see also XTAL1). XTAL2 is used as a crystal oscillator output or buffered a clock output.

Detailed Description

Hardware Autoflow Control (see Figure 1)

Hardware autoflow control is comprised of auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$. With auto-$\overline{\text{CTS}}$, the $\overline{\text{CTS}}$ input must be active before the transmitter FIFO can emit data. With auto-$\overline{\text{RTS}}$, $\overline{\text{RTS}}$ becomes active when the receiver needs more data and notifies the sending serial device. When $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using ACE1 and ACE2 from a TLC16C2752 with the autoflow control enabled. If not, overrun errors can occur when the transmit data rate exceeds the receiver FIFO read latency.

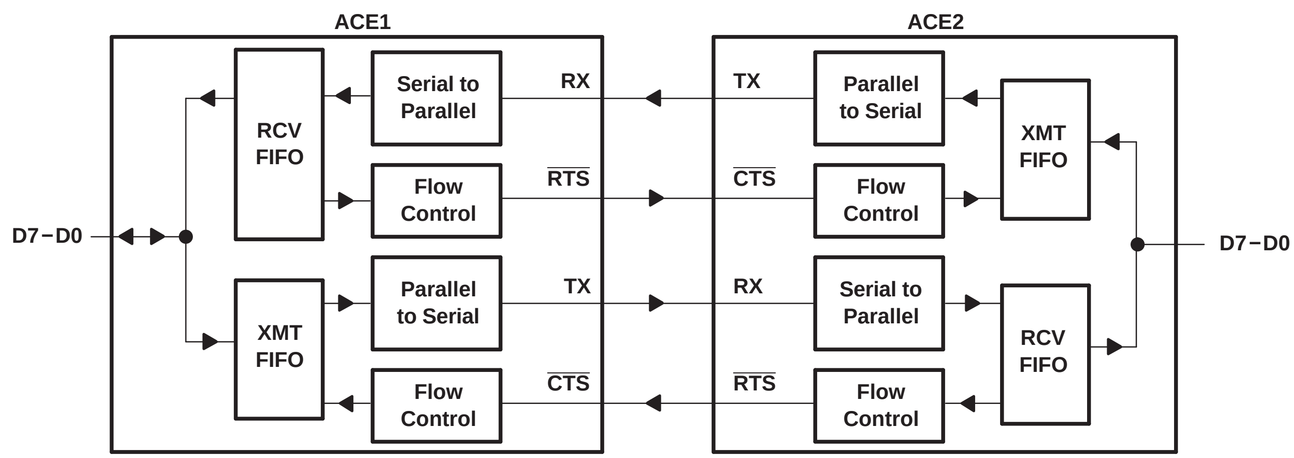


Figure 1. Autoflow Control (Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$) Example

Auto-$\overline{\text{RTS}}$

Auto-$\overline{\text{RTS}}$ data flow control originates in the receiver timing and control block (see Figure 4) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches the defined halt trigger level 8 (see Figure 3), $\overline{\text{RTS}}$ is deasserted. The sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{\text{RTS}}$ until after it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the defined resume trigger level is reached.

Auto-$\overline{\text{CTS}}$

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte. When $\overline{\text{CTS}}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 2). The auto-$\overline{\text{CTS}}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{\text{CTS}}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$ Functional Timing

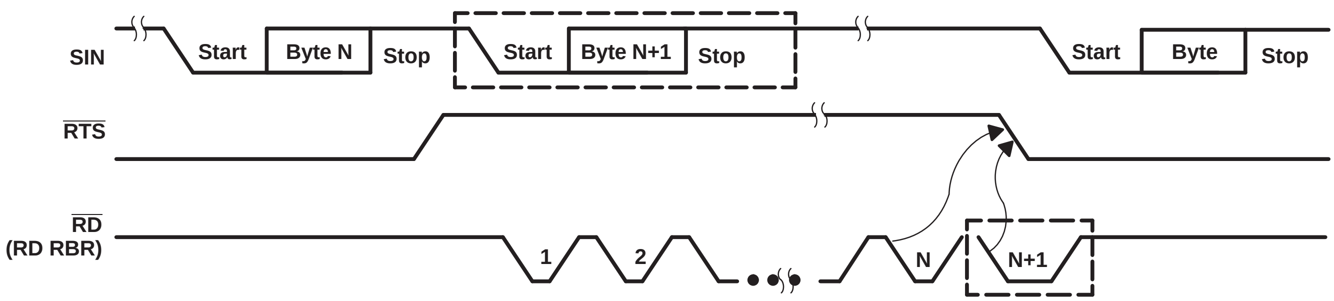


Figure 2. $\overline{\text{RTS}}$ Functional Timing Waveforms

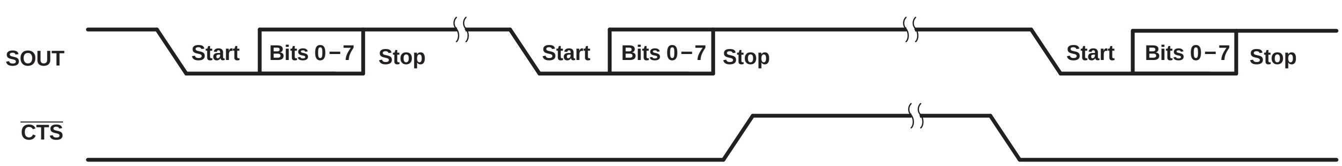


Figure 3. $\overline{\text{CTS}}$ Functional Timing Waveforms

A. Pin numbers shown are for 44-pin PLCC FN package.

Figure 4. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		–0.5	7	V
V_I	Input voltage range at any input		–0.5	7	V
V_O	Output voltage range		–0.5	7	V
T_A	Operating free-air temperature range	TL16C2752	0	70	°C
		TL16C2752I	–40	85	
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS
1.8 V = 10%

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	1.62	1.8	1.98	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	High-level input voltage	1.4		1.98	V
V_{IL}	Low-level input voltage	–0.3		0.4	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current (all outputs)			0.5	mA
I_{OL}	Low-level output current (all outputs)			1	mA
	Oscillator/clock speed			10	MHz

RECOMMENDED OPERATING CONDITIONS
2.5 V = 10%

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.25	2.5	2.75	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	High-level input voltage	1.8		2.75	V
V_{IL}	Low-level input voltage	–0.3		0.6	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current (all outputs)			1	mA
I_{OL}	Low-level output current (all outputs)			2	mA
	Oscillator/clock speed			16	MHz

RECOMMENDED OPERATING CONDITIONS
3.3 V = 10%

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	High-level input voltage	$0.7 \times V_{CC}$			V
V_{IL}	Low-level input voltage			$0.3 \times V_{CC}$	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current (all outputs)			1.8	mA
I_{OL}	Low-level output current (all outputs)			3.2	mA
	Oscillator/clock speed			20	MHz

RECOMMENDED OPERATING CONDITIONS
5 V = 10%

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage	All except XTAL1, XTAL2	2			V
		XTAL1, XTAL2	$0.7 \times V_{CC}$			
V_{IL}	Low-level input voltage	All except XTAL1, XTAL2			0.8	V
		XTAL1, XTAL2			$0.3 \times V_{CC}$	
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current (all outputs)				4	mA
I_{OL}	Low-level output current (all outputs)				4	mA
	Oscillator/clock speed				24	MHz

ELECTRICAL CHARACTERISTICS
1.8 V Nominal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage(2)	I_{OH} = –0.5 mA	1.3			V
V_{OL}	Low-level output voltage(2)	I_{OL} = 1 mA			0.5	V
I_I	Input current	V_{CC} = 1.98 V, V_{SS} = 0, V_I = 0 to 1.98 V, All other terminals floating			10	= A
I_{OZ}	High-impedance-state output current	V_{CC} = 1.98 V, V_{SS} = 0, V_I = 0 to 1.98 V, Chip selected in write mode or chip deselected			±20	= A
I_{CC}	Supply current	V_{CC} = 1.98 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 1.4 V, All other inputs at 0.4 V, XTAL1 at 16 MHz, No load on outputs				mA
$C_{i(CLK)}$	Clock input impedance			15	20	pF
$C_{O(CLK)}$	Clock output impedance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		20	30	pF
C_I	Input impedance			6	10	pF
C_O	Output impedance			10	20	pF

(1) All typical values are at V_{CC} = 1.8 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.

ELECTRICAL CHARACTERISTICS
2.5 V Nominal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage(2)	I_{OH} = –1 mA	1.8			V
V_{OL}	Low-level output voltage(2)	I_{OL} = 2 mA			0.5	V
I_I	Input current	V_{CC} = 2.75 V, V_{SS} = 0, V_I = 0 to 2.75 V, All other terminals floating			10	= A
I_{OZ}	High-impedance-state output current	V_{CC} = 2.75 V, V_{SS} = 0, V_I = 0 to 2.75 V, Chip selected in write mode or chip deselected			±20	= A
I_{CC}	Supply current	V_{CC} = 2.75 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 1.8 V, All other inputs at 0.6 V, XTAL1 at 24 MHz, No load on outputs				mA
$C_{i(CLK)}$	Clock input impedance			15	20	pF
$C_{O(CLK)}$	Clock output impedance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		20	30	pF
C_I	Input impedance			6	10	pF
C_O	Output impedance			10	20	pF

(1) All typical values are at V_{CC} = 2.5 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.

ELECTRICAL CHARACTERISTICS
3.3 V Nominal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage(2)	I_{OH} = –1.8 mA	2.4			V
V_{OL}	Low-level output voltage(2)	I_{OL} = 3.2 mA			0.5	V
I_I	Input current	V_{CC} = 3.6 V, V_{SS} = 0, V_I = 0 to 3.6 V, All other terminals floating			10	= A
I_{OZ}	High-impedance-state output current	V_{CC} = 3.6 V, V_{SS} = 0, V_I = 0 to 3.6 V, Chip selected in write mode or chip deselected			±20	= A
I_{CC}	Supply current	V_{CC} = 3.6 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 2 V, All other inputs at 0.8 V, XTAL1 at 32 MHz, No load on outputs				mA
$C_{i(CLK)}$	Clock input impedance			15	20	pF
$C_{O(CLK)}$	Clock output impedance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		20	30	pF
C_I	Input impedance			6	10	pF
C_O	Output impedance			10	20	pF

(1) All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.

ELECTRICAL CHARACTERISTICS
5 V Nominal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage(2)	I_{OH} = –4 mA	4			V
V_{OL}	Low-level output voltage(2)	I_{OL} = 4 mA			0.4	V
I_I	Input current	V_{CC} = 5.5 V, V_{SS} = 0, V_I = 0 to 5.5 V, All other terminals floating			10	= A
I_{OZ}	High-impedance-state output current	V_{CC} = 3.6 V, V_{SS} = 0, V_I = 0 to 3.6 V, Chip selected in write mode or chip deselected			= 20	= A
I_{CC}	Supply current	V_{CC} = 5.5 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 2 V, All other inputs at 0.8 V, XTAL1 at 32 MHz, No load on outputs				mA
$C_{i(CLK)}$	Clock input impedance			15	20	pF
$C_{O(CLK)}$	Clock output impedance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		20	30	pF
C_I	Input impedance			6	10	pF
C_O	Output impedance			10	20	pF

(1) All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS 1.8 V MIN	1.8 V MAX	2.5 V MIN	2.5 V MAX	3.3 V MIN	3.3 V MAX	5 V MIN	5 V MAX	UNIT
t_{w8}	Pulse duration, RESET	t_{RESET}			1		1		1		1		= s
t_{w1}	Pulse duration, clock high	t_{XH}	6		25		16		12		8		ns
t_{w2}	Pulse duration, clock low	t_{XL}											
t_{cR}	Cycle time, read (t_{w7} + t_{d8} + t_{h7})	RC	8		115		80		62		57		ns
t_{cW}	Cycle time, write (t_{w6} + t_{d5} + t_{h4})	WC	7		115		80		62		57		ns
t_{w6}	Pulse duration, $\overline{IOW}$ or $\overline{CS}$	t_{IOW}	7		80		55		45		40		ns
t_{w7}	Pulse duration, $\overline{IOR}$ or $\overline{CS}$	t_{IOR}	8		80		55		45		40		ns
t_{SU3}	Setup time, data valid before $\overline{IOW}$↑ or $\overline{CS}$↑	t_{DS}	7		25		20		15		15		ns
t_{h4}	Hold time, address valid after $\overline{IOW}$↑ or $\overline{CS}$↑	t_{WA}	7		20		15		10		10		ns
t_{h5}	Hold time, data valid after $\overline{IOW}$↑ or $\overline{CS}$↑	t_{DH}	7		15		10		5		5		ns
t_{h7}	Hold time, data valid after $\overline{IOR}$↑ or $\overline{CS}$↑	t_{RA}	8		20		15		10		10		ns
t_{d5}	Delay time, address valid before $\overline{IOW}$↓ or $\overline{CS}$↓	t_{AW}	7		15		10		7		7		ns
t_{d8}	Delay time, address valid to $\overline{IOR}$↓ or $\overline{CS}$↓	t_{AR}	8		15		10		7		7		ns
t_{d10}	Delay time, $\overline{IOR}$↓ or $\overline{CS}$↓ to data valid	t_{RVD}	8	C_L = 30 pF		55		35		25		20	ns
t_{d11}	Delay time, $\overline{IOR}$↑ or $\overline{CS}$↑ to floating data	t_{HZ}	8	C_L = 30 pF		40		30		20		20	ns
t_{d12}	Write cycle to write cycle delay		7			100		75		60		50	ns
t_{d13}	Read cycle to read cycle delay		8			100		75		60		50	ns

BAUD GENERATOR SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (for FN package only)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS								UNIT
					1.8 V		2.5 V		3.3 V		5 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{w3}	Pulse duration, $\overline{\text{BAUDOUT}}$ low	t_{LW}	6	CLK ÷ 2	50		35		27		16		ns
t_{w4}	Pulse duration, $\overline{\text{BAUDOUT}}$ high	t_{HW}	6	CLK ÷ 2	50		35		27		16		ns
t_{d1}	Delay time, XIN↑ to $\overline{\text{BAUDOUT}}$↑	t_{BLD}	6			35		25		20		15	ns
t_{d2}	Delay time, XIN↑↓ to $\overline{\text{BAUDOUT}}$↓	t_{BHD}	6			35		25		20		15	ns

RECEIVER SWITCHING CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS								UNIT
					1.8 V		2.5 V		3.3 V		5 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{d12}	Delay time, RCLK to sample	t_{SCD}	9			20		15		10		10	ns
t_{d13}	Delay time, stop to set INT or read $\overline{\text{RBR}}$ to LSI interrupt or stop to $\overline{\text{RXRDY}}$↓	t_{SINT}	8, 9, 10, 11, 12			1		1		1	1		RCLK cycle
t_{d14}	Delay time, read RBR/LSR to reset INT	t_{RINT}	8, 9, 10, 11, 12	C_L = 30 pF		100		90		80		70	ns
t_{d26}	Delay time, RCV threshold byte to $\overline{\text{RTS}}$↑		19	C_L = 30 pF								2	baudout cycles(2)
t_{d27}	Delay time, read of last byte in receive FIFO to $\overline{\text{RTS}}$↓		19	C_L = 30 pF								2	baudout cycles
t_{d28}	Delay time, first data bit of 16th character to $\overline{\text{RTS}}$↑		20	C_L = 30 pF								2	baudout cycles
t_{d29}	Delay time, $\overline{\text{RBRRD}}$ low to $\overline{\text{RTS}}$↓		20	C_L = 30 pF								2	baudout cycles

(1) In the FIFO mode, the read cycle (RC) = 1 baud clock (min) between reads of the receive FIFO and the status registers (interrupt identification register or line status register).
(2) A baudout cycle is equal to the period of the input clock divided by the programmed divider in DLL, DLM.

TRANSMITTER SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS								UNIT
					1.8 V		2.5 V		3.3 V		5 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{d15}	Delay time, initial write to transmit start	t_{IRS}	14		8	24	8	24	8	24	8	24	baudout cycles
t_{d16}	Delay time, start to INT	t_{STI}	14		8	10	8	10	8	10	8	10	baudout cycles
t_{d17}	Delay time, $\overline{\text{IOW}}$ (WR THR) to reset INT	t_{HR}	14	C_L = 30 pF		70		60		50		50	ns
t_{d18}	Delay time, initial write to INT (THRE(1))	t_{SI}	14		16	34	16	34	16	34	16	34	baudout cycles
t_{d19}	Delay time, read $\overline{\text{IOR}}$↑ to reset INT (THRE(1))	t_{IR}	14	C_L = 30 pF		70		50		35		35	ns
t_{d20}	Delay time, write to $\overline{\text{TXRDY}}$ inactive	t_{WXI}	15, 16	C_L = 30 pF		60		45		35		35	ns
t_{d21}	Delay time, start to $\overline{\text{TXRDY}}$ active	t_{SXA}	15, 16	C_L = 30 pF		9		9		9		9	baudout cycles
t_{SU4}	Setup time, $\overline{\text{CTS}}$↑ before midpoint of stop bit		18		30		20		10		10		ns
t_{d25}	Delay time, $\overline{\text{CTS}}$ low to TX↓		18	C_L = 30 pF		24		24		24		24	baudout cycles

(1) THRE = Transmitter holding register empty; IIR = interrupt identification register

MODEM CONTROL SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS 1.8 V MIN	LIMITS 1.8 V MAX	2.5 V MIN	2.5 V MAX	3.3 V MIN	3.3 V MAX	5 V MIN	5 V MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	17	C_L = 30 pF		90		70		60		50	ns
t_{d23}	Delay time, modem interrupt to set INT	t_{SIM}	17	C_L = 30 pF		60		50		40		35	ns
t_{d24}	Delay time, RD MSR to reset INT	t_{RIM}	17	C_L = 30 pF		80		60		50		40	ns

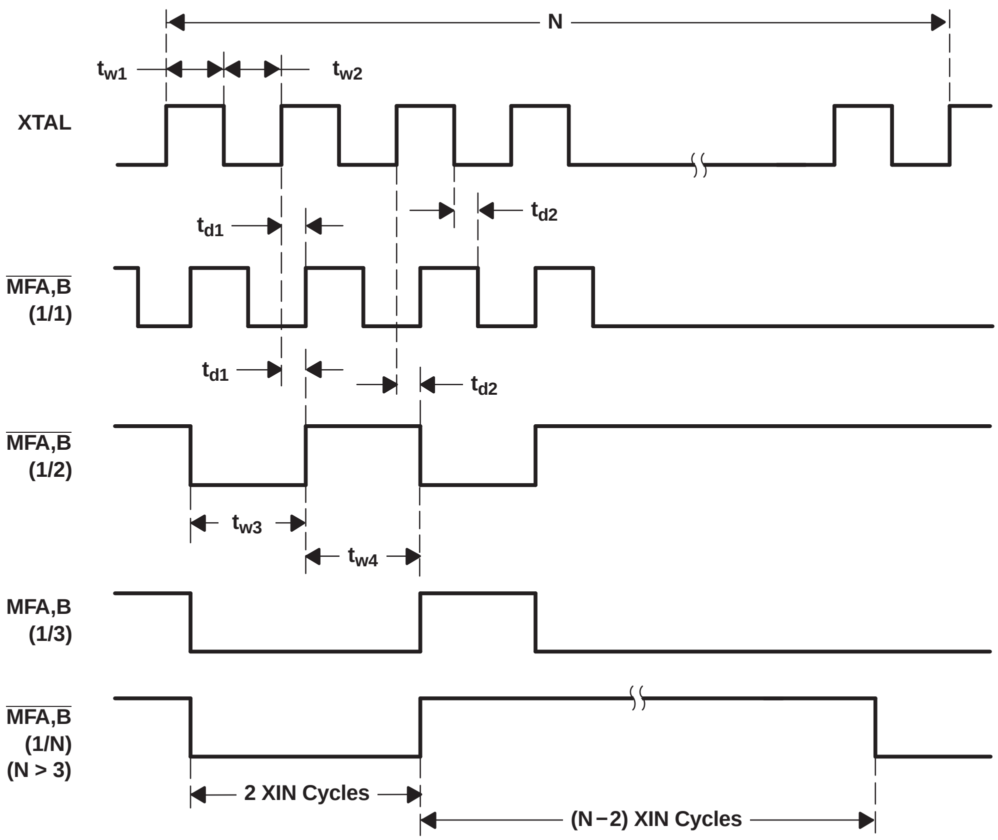


Figure 5. Input Clock and Baud Generator Timing Waveforms (for FN Package Only) (When AFR2:1 = 01)

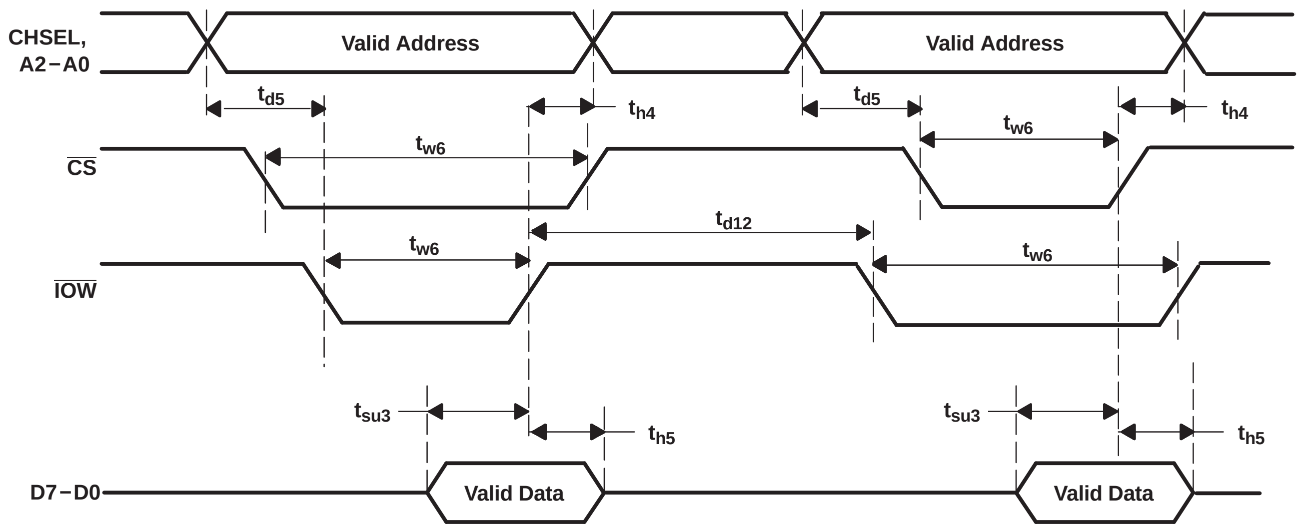


Figure 6. Write Cycle Timing Waveforms

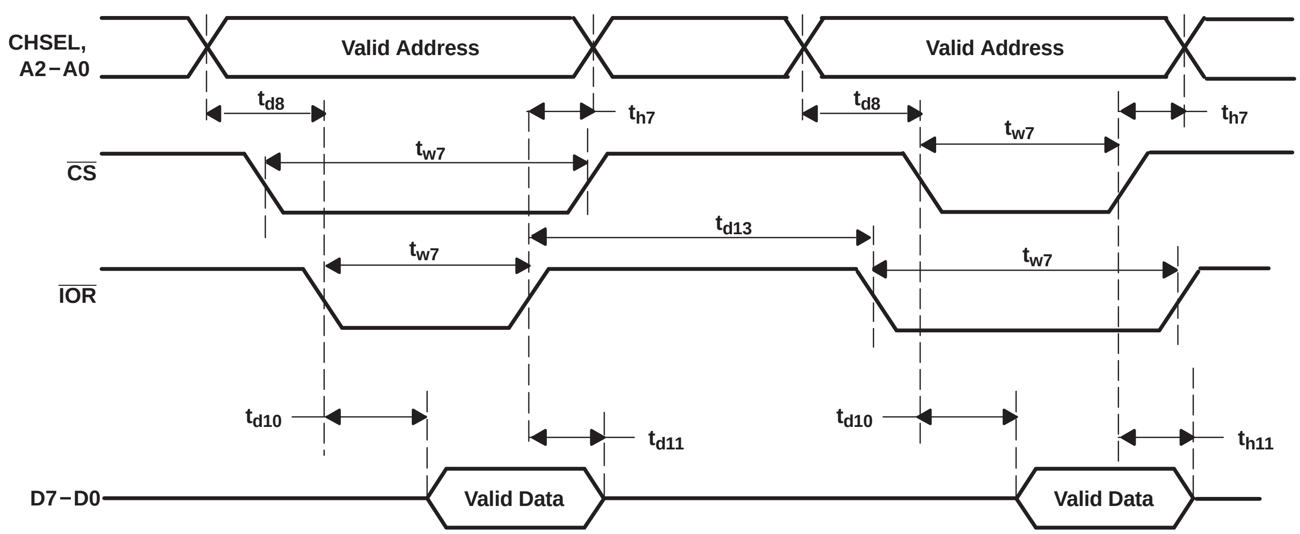


Figure 7. Read Cycle Timing Waveforms

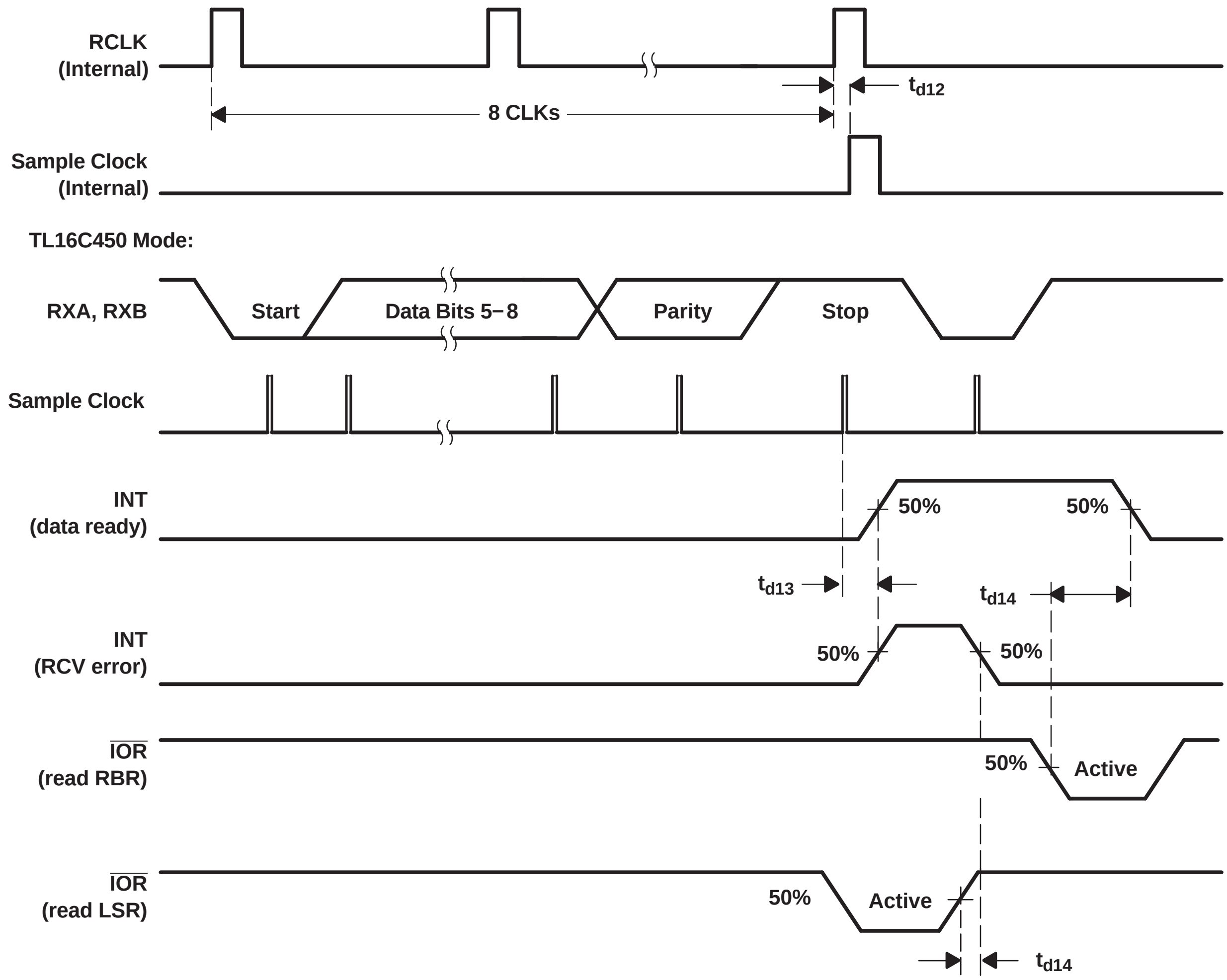


Figure 8. Receiver Timing Waveforms

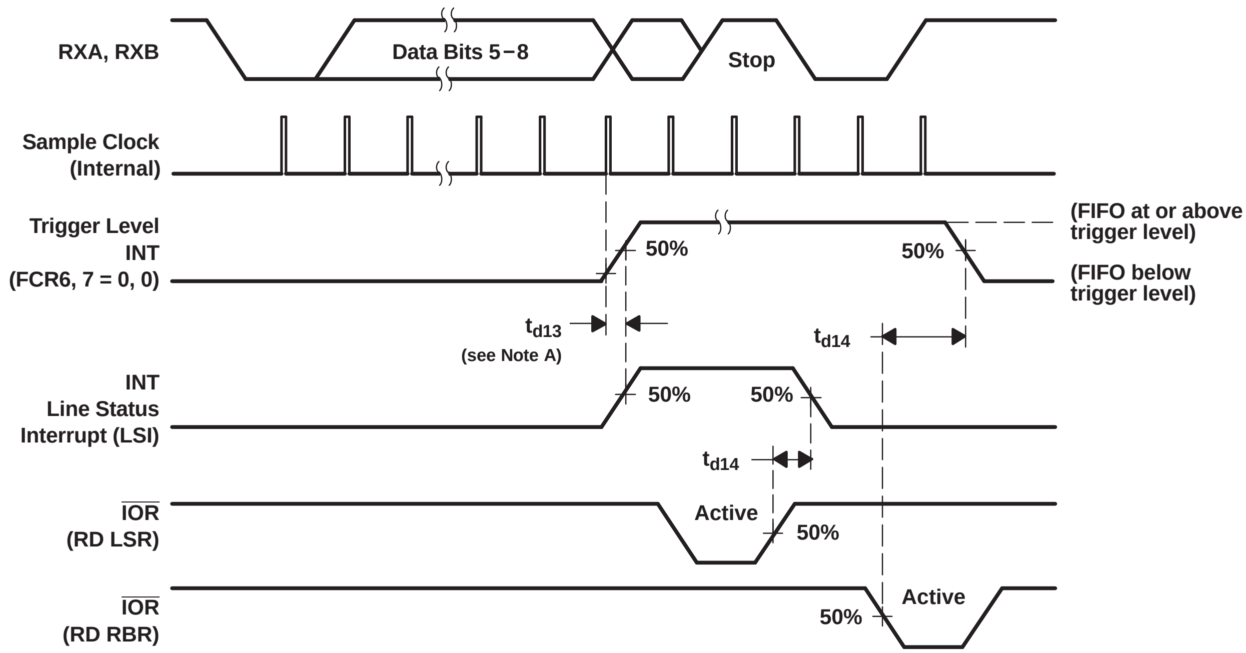


Figure 9. Receive FIFO First Byte (Sets DR Bit) Waveforms

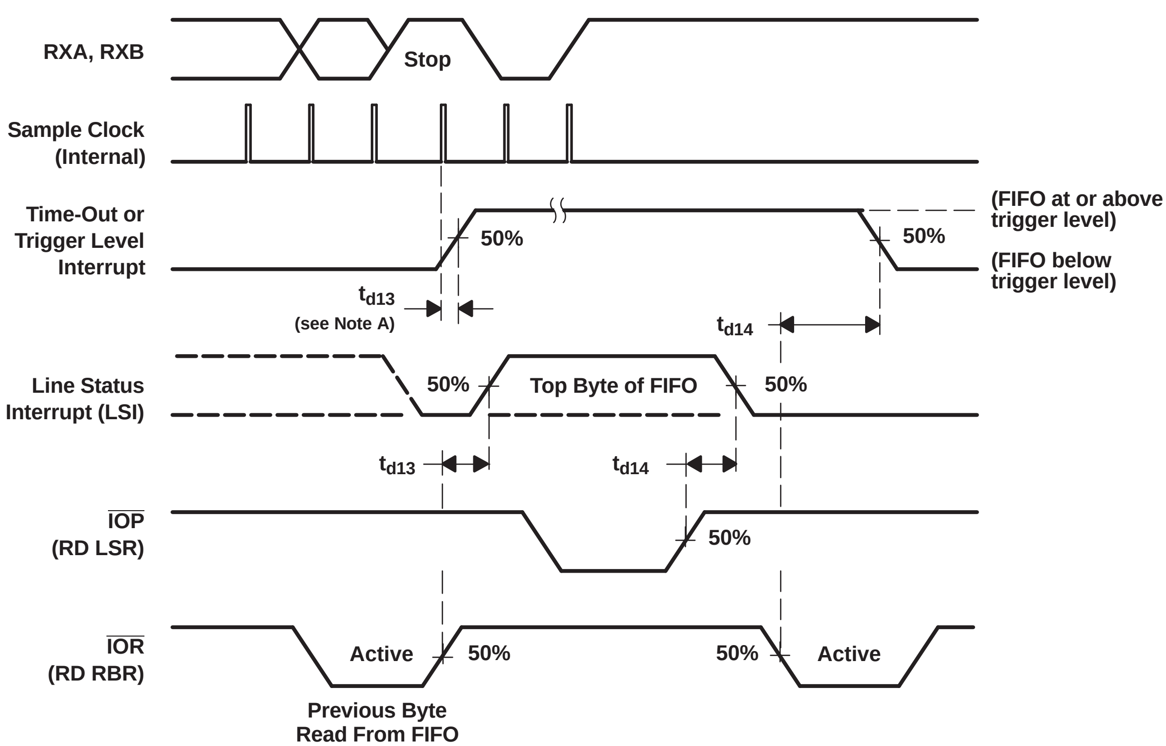


Figure 10. Receive FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

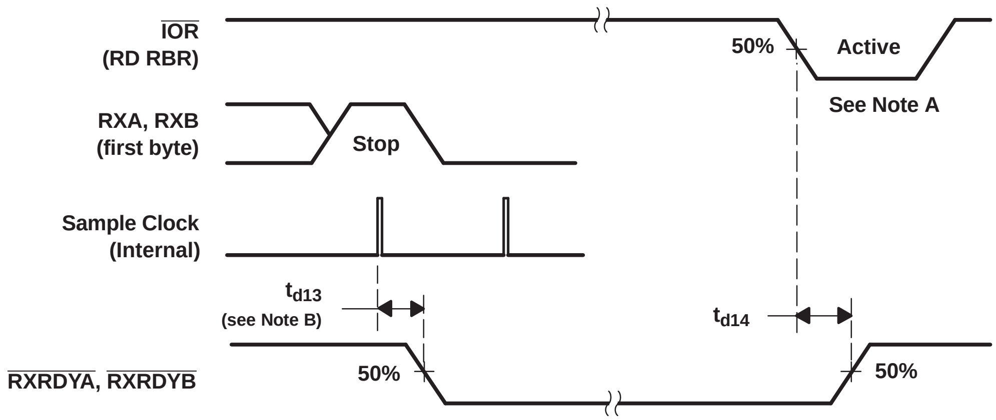


Figure 11. Receiver Ready (RXRDY) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

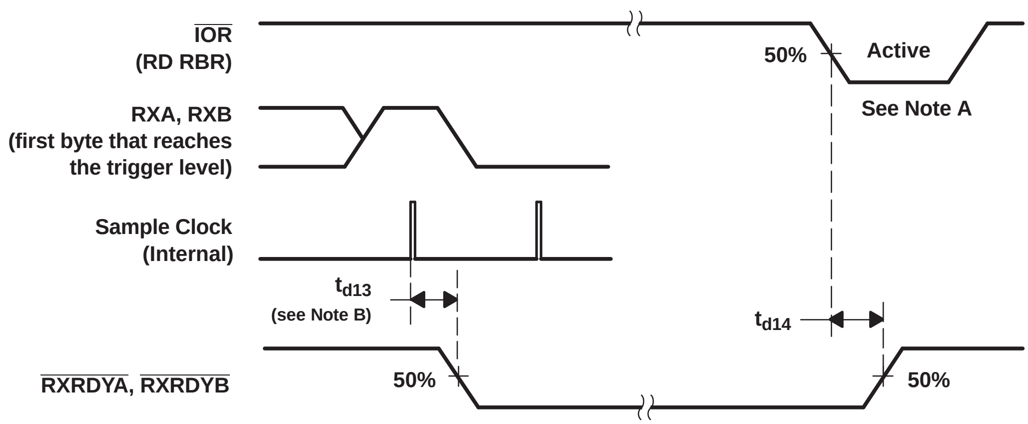


Figure 12. Receiver Ready (RXRDY) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

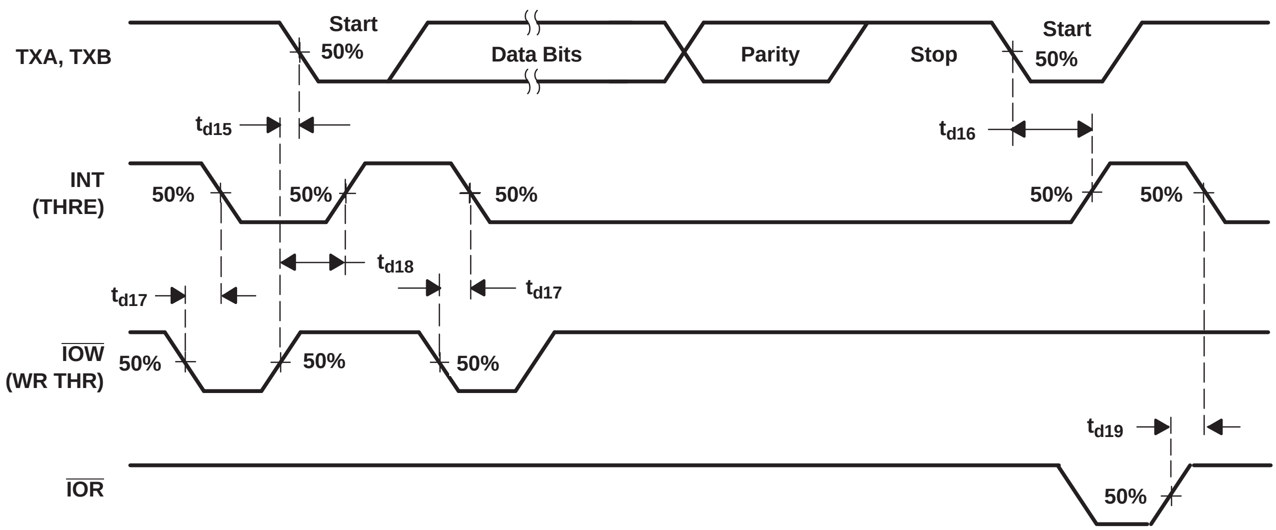


Figure 13. Transmitter Timing Waveforms

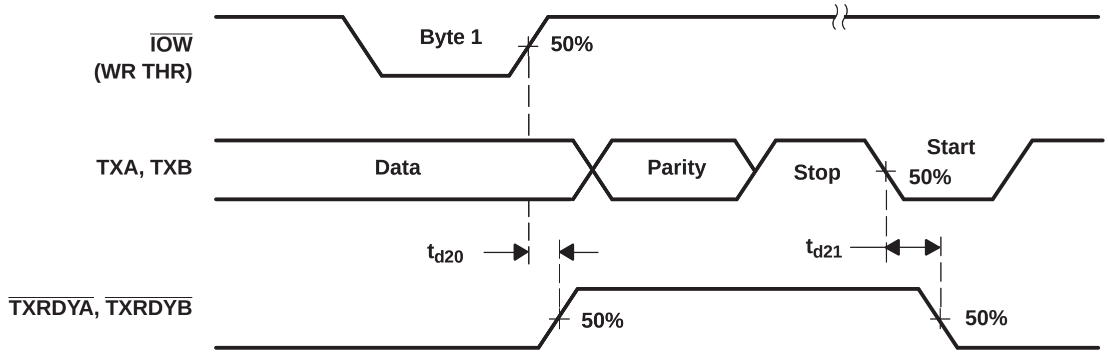


Figure 14. Transmitter Ready (TXRDY) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

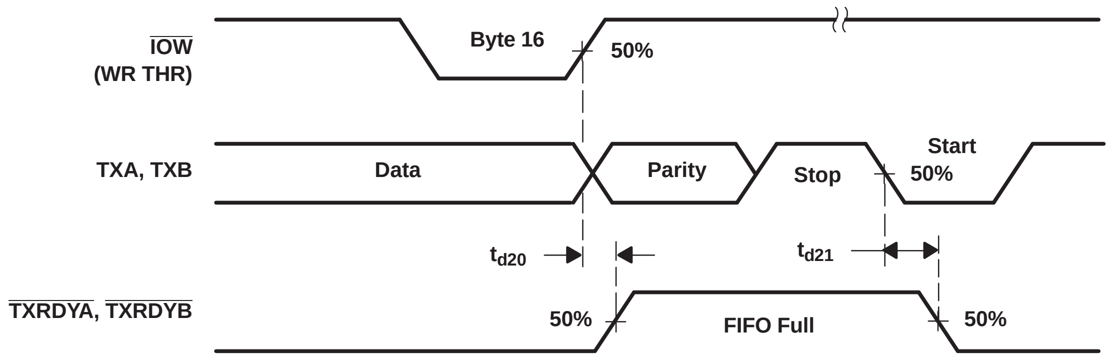


Figure 15. Transmitter Ready (TXRDY) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

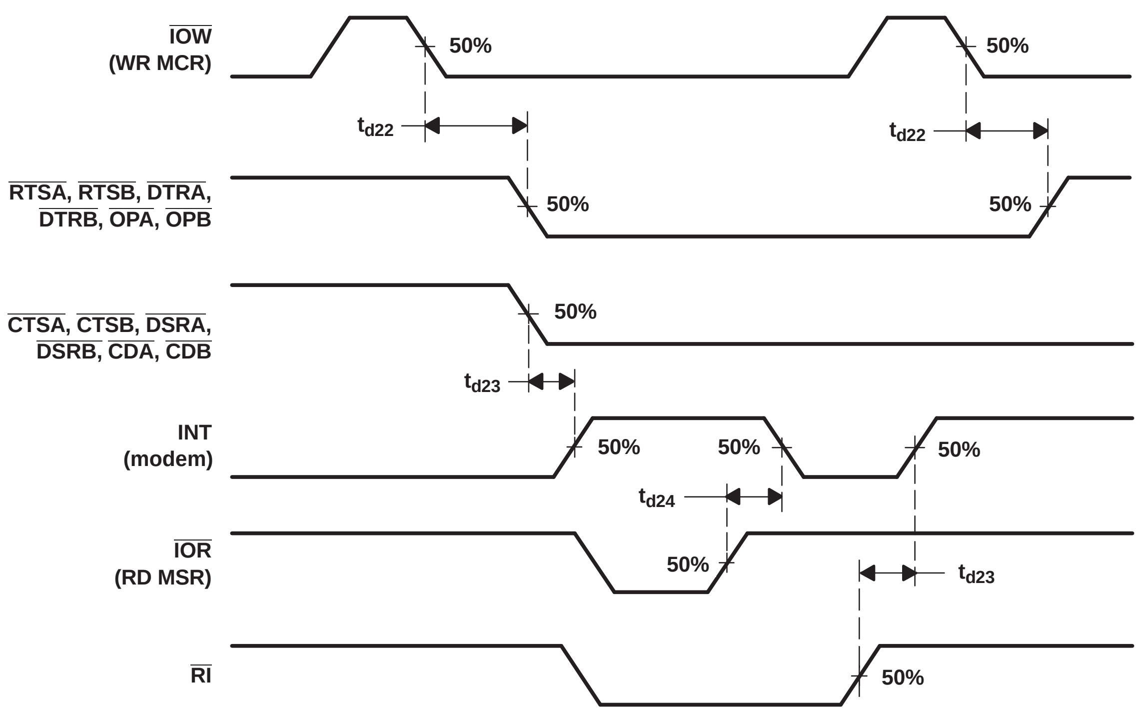


Figure 16. Modem Control Timing Waveforms

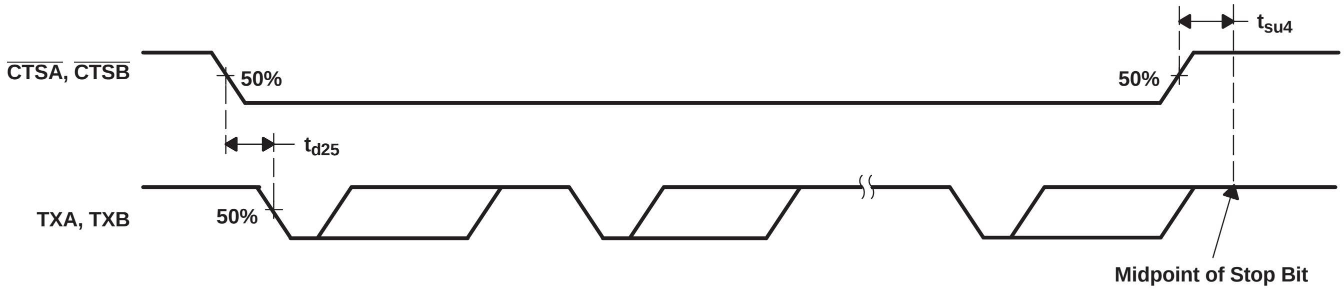


Figure 17. CTS and TX Autoflow Control Timing (Start and Stop) Waveforms

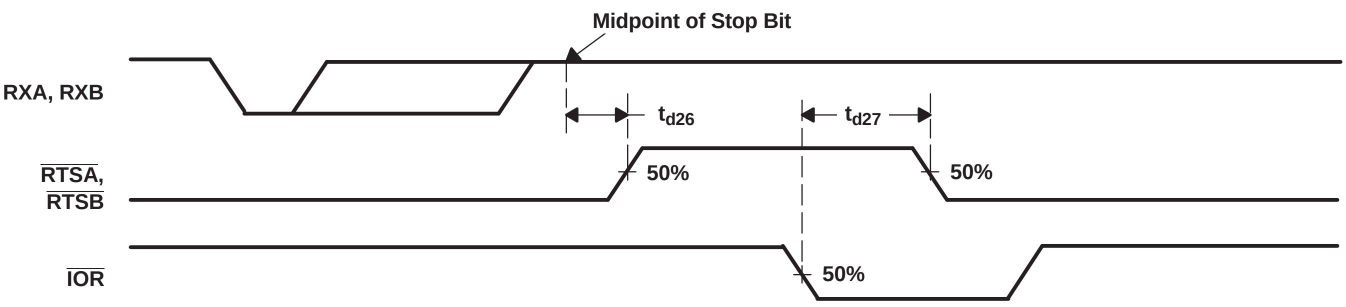


Figure 18. Auto-RTS Timing

APPLICATION INFORMATION

A. Pin numbers shown are for 44-pin PLCC FN package.

Figure 19. Typical TL16C2752 Connection

PRINCIPLES OF OPERATION

UART Internal Registers

Each of the UART channel in the TL16C2752 has its own set of configuration registers selected by address lines A0, A1, and A2 with $\overline{CS}$ and CHSEL selecting the channel. The complete register set is shown in Table 1 and Table 2.

Table 1. UART Channel A and B UART Internal Registers

ADDRESS A2–A0	RESET (HEX) VALUE	COMMENTS	REGISTER	READ/WRITE
16C550 Compatible Registers				
0 0 0	XX XX	LCR[7] = 0	RHR–Receive Holding Register THR–Transmit Holding Register	Read only Write only
0 0 0	XX	LCR[7] = 1, LCR ≠ 0xBF	DLL–Div Latch Low Byte	Read/Write
0 0 1	XX		DLM–Div Latch High Byte	Read/Write
0 1 0	00		AFR–Alternate Function Register	Read/Write
0 0 0	00	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF	DREV–Device Revision Code	Read only
0 0 1	0A		DVID–Device Identification Code	Read only
0 0 1	00	LCR[7] = 0	IER–Interrupt Enable Register	Read/Write
0 1 0	01 00	LCR[7] = 0	ISR–Interrupt Status Register FCR–FIFO Control Register	Read only Write only
0 1 1	00		LCR–Line Control Register	Read/Write
1 0 0	00	LCR ≠ 0xBF	MCR–Modem Control Register	Read/Write
1 0 1	60		LSR–Line Status Register Reserved	Read only Write only
1 1 0	X0		MSR–Modem Status Register Reserved	Read only Write only
1 1 1	FF	LCR ≠ 0xBF, FCTR[6] = 0	SPR–Scratch Pad Register	Read/Write
1 1 1	00	LCR ≠ 0xBF, FCTR[6] = 1	FLVL–RX/TX FIFO Level Counter Register	Read only
1 1 1	80		EMSR–Enhanced Mode Select Register	Write only
Enhanced Registers				
0 0 0	00 00	LCR = 0xBF	TRG–RX/TX FIFO Trigger Level Register FC–RX/TX FIFO Level Counter Register	Write only Read only
0 0 1	00		FCTR–Feature Control Register	Read/Write
0 1 0	00		EFR–Enhanced Function Register	Read/Write
1 0 0	00		Xon-1–Xon Character 1	Read/Write
1 0 1	00		Xon-2–Xon Character 2	Read/Write
1 1 0	00		Xoff-1–Xoff Character 1	Read/Write
1 1 1	00		Xoff-2–Xoff Character 2	Read/Write

Table 2. Internal Registers Description(1)

Address A2–A0	Register Name	Read/ Write	Comments	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16C550 Compatible Registers											
0 0 0	RHR	RD	LCR[7] = 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 0 0	THR	WR		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 0 1	IER	RD/WR		0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int. Enable	RX Data Int. Enable
0 1 0	ISR	RD		FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit 5	0/ INT Source Bit 4	INT Source Bit 3	INT Source Bit 2	INT Source Bit 1	INT Source Bit 0
0 1 0	FCR	WR		RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable
0 1 1	LCR	RD/WR	LCR ≠ 0xBF	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit 1	Word Length Bit 0
1 0 0	MCR	RD/WR		0/ BRG Prescaler	0/ IR Mode Enable	0/ XonAny	Internal Loopback Enable	OP2# Output Control	Rsrvd (OP1#)	RTS# Output Control	DTR# Output Control
1 0 1	LSR	RD		RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Overrun Error	RX Data Ready
1 1 0	MSR	RD		CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#
1 1 1	SPR	RD/WR	LCR ≠ 0xBF FCTR Bit 6 = 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 1 1	EMSR	WR	LDR ≠ 0xBF FCTR Bit 6 = 1	16X Sampling Rate Mode	LSR Error Interrupt Imd/Dly#	Auto RTS Hyst. Bit 3	Auto RTS Hyst Bit 2	Auto RS485 Output Inversion	Rsrvd	Rx/Tx FIFO Count	Rx/Tx FIFo Count
1 1 1	FLVL	RD		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Baud-Rate Generator Divisor											
0 0 0	DLL	RD/WR	LCR[7] = 1 LCR ≠ 0xBF	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 0 1	DLM	RD/WR		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 1 0	AFR	RD/WR		Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	RXRDY# Select	Baudout# Select	Concurrent Write
0 0 0	DREV	RD	LCR[7] = 1 LCR ≠ 0xBF DLL = 0x00 DLM = 0x00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 0 1	DVID	RD		0	0	0	0	1	0	1	0
Enhanced Registers											
0 0 0	TRG	WR	LCR = 0xBF	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 0 0	FC	RD		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 0 1	FCTR	RD/WR		RX/TX Mode	SCPAD Swap	Trig Table Bit 1	Trig Table Bit 0	Auto RS485 Direction Control	RX IR Input Inv.	Auto RTS Hyst Bit 1	Auto RTS Hyst Bit 0
0 1 0	EFR	RD/WR		Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER[7:4], ISR[5:4], FCT[5:4], MCR[7:5]	Software Flow Cntl Bit 3	Software Flow Cntl Bit 2	Software Flow Cntl Bit 1	Software Flow Cntl Bit 0
1 0 0	XON1	RD/WR		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 0 1	XON2	RD/WR		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 1 0	XOFF1	RD/WR		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 1 1	XOFF2	RD/WR		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

(1) Shaded bits are accessible when EFR Bit 4 = 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL16C2752FN	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16C2752FNG4	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16C2752FNR	ACTIVE	PLCC	FN	44	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16C2752FNRG4	ACTIVE	PLCC	FN	44	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16C2752IFN	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16C2752IFNG4	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16C2752IFNR	ACTIVE	PLCC	FN	44	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16C2752IFNRG4	ACTIVE	PLCC	FN	44	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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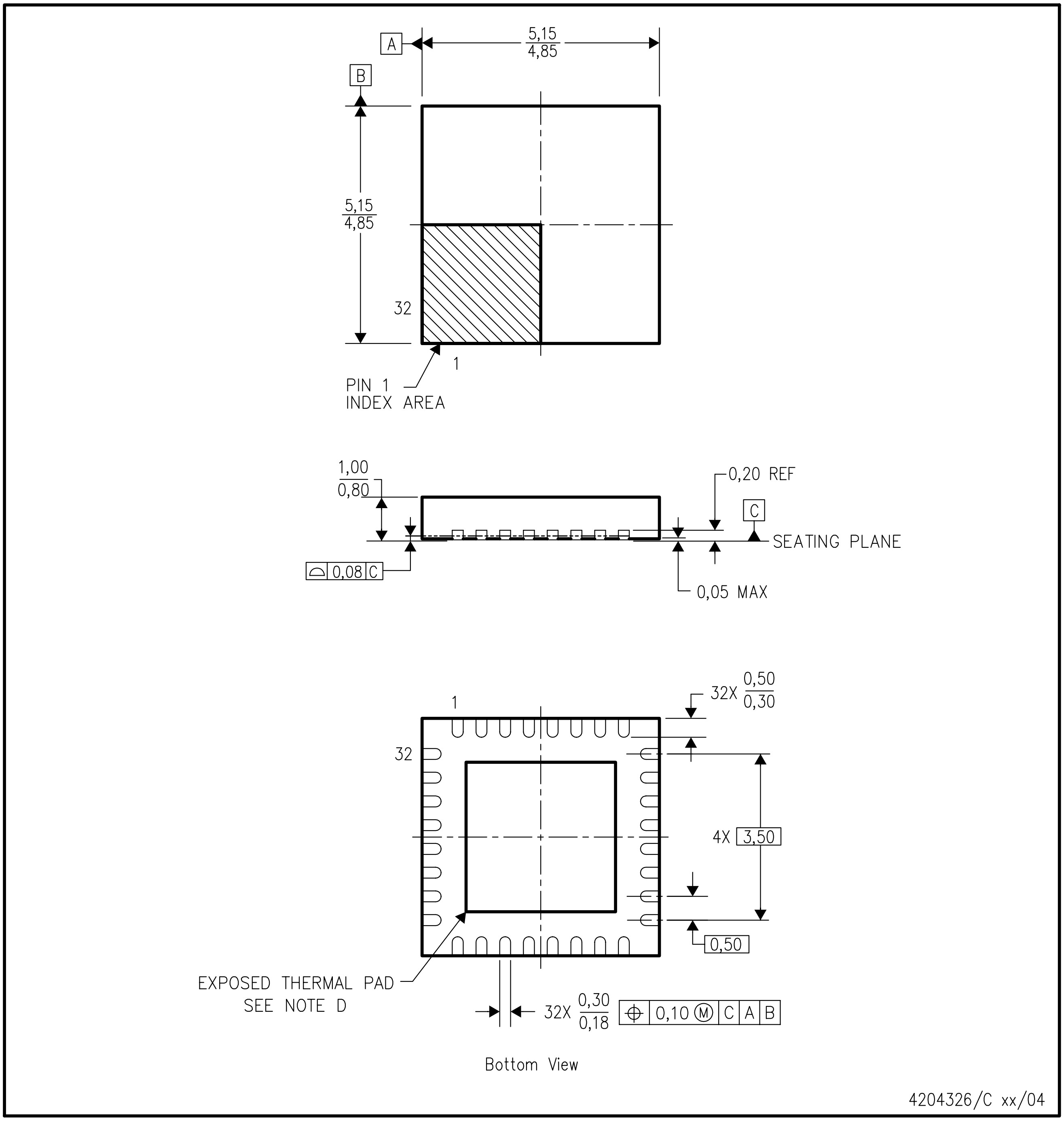
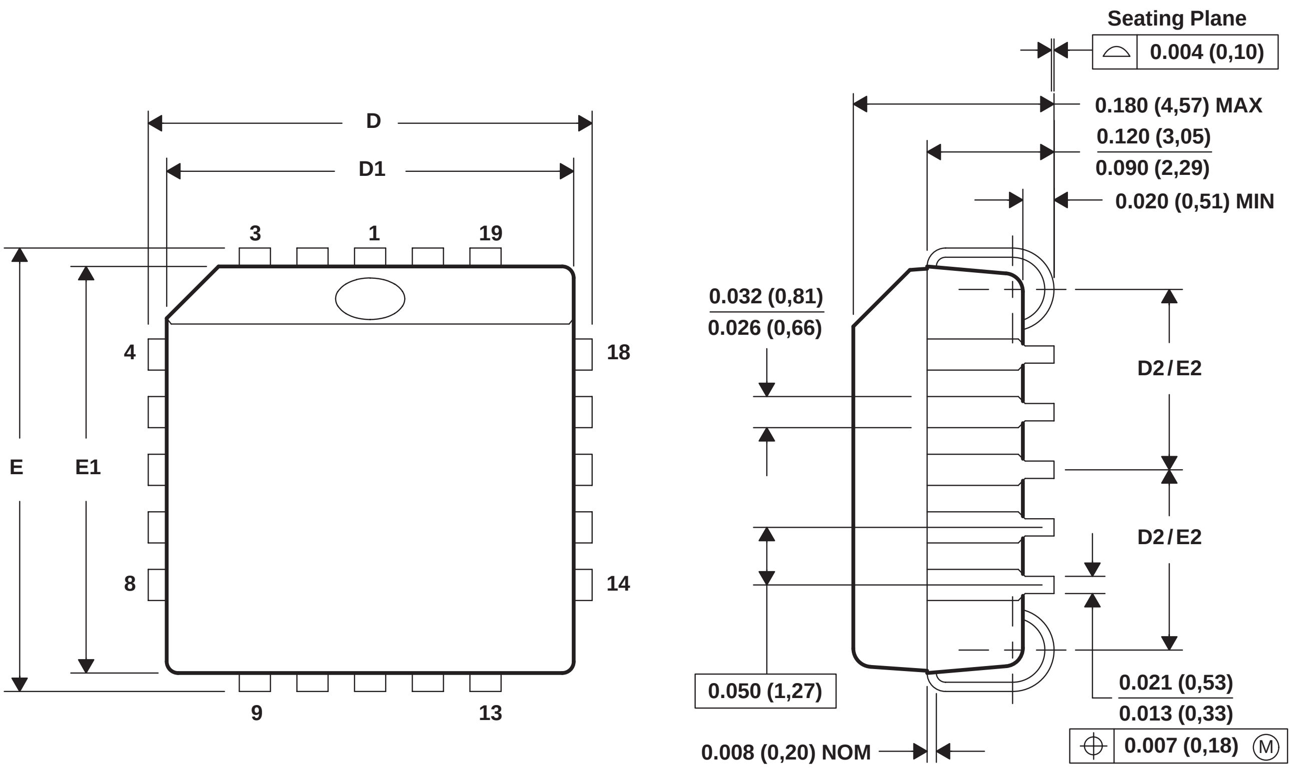
RHB (S-PQFP-N32) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018